



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor

Satoshi IDE

Shinichi SAKURAMOTO

Serial No.

09/478,604

Filed

January 6, 2000

Title

BURST SIGNAL DETECTION CIRCUIT

Examiner

Augustin Bello

Group Art Unit

2633

April 12, 2004

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450 RECEIVED

APR 1 9 2004

Technology Center 2600

TÖ RESTRICTION REOUIREMENT

Sir:

In response to the Restriction Requirement mailed on March 10, 2004, Applicants elect without traverse a claim grouping associated with a first species of invention described by Figures 1, 2A-2C and 3A-3B. Applicants submit that claims 1, 2, 4, 8-11, 13, 17, 19, 22,26, 27, 28., 34, 38 and 39 read on the elected species.

Applicants reserve all rights to file one or more divisional patent applications based on the unelected claims at a future time.

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Receipt No. £ 979,34802 45

An earnest effort has been made to respond to this Restriction Requirement. It is believed that elected claims 1, 2, 4, 8-11, 13, 17, 19, 22, 26, 27, 28, 34, 38 and 39 stand in condition for allowance. Passage of this application to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further action.

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Respectfully submitted,

Thomas J. Bean Reg. No. 44,528

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